# DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

**LAB MANUAL**

**FOR**

# MINE ELECTRONICS LAB


**Lab Manual Designed By**

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**MALLA REDDY ENGINEERING COLLEGE**
**(AUTONOMOUS)**

**NAAC accredited with 'A' Grade**
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# IMPORTANCE OF EDC LAB

*"A practical approach is probably the best approach to mastering a subject and gaining a clear insight."*

Electronic Devices and Circuits lab covers those practical oriented Electronic circuits that are very essential for the students to solidify their theoretical concepts. This provides a communication bridge between the theory and practical world of the electronic circuits. The knowledge of these practical are very essential for the engineering students. All of these practical are arranged on the modern electronic trainer boards.

The lab section consists of Diode circuits. Some of the very useful diode based circuits. Labs concerning over this part provides the elementary knowledge of the subject. It also provides some sort of introduction to the lab equipments. This lab also describes the Bipolar Junction Transistor based circuits. Different configurations of BJT amplifier are discussed in this part of the book .Each and every practical provides a great in depth practical concepts of BJT. It also covers some other useful features such as biasing concepts, different type of biasing technique and load line concept, Oscillators and Feedback amplifiers etc. And this lab consists of Field Effect Transistor (FET); one of the leading technologies in electronics is discussed. It gives the introduction to the FET based electronic circuits.

# ELECTRONIC DEVICES AND CIRCUITS LAB

# 1. FORWARD & REVERSE BIAS CHARACTERISTICS OF PN JUNCTION DIODE

**AIM:-** 1. To Plot the Volt -Ampere Characteristics of PN Junction diode under Forward and Reverse bias Conditions.

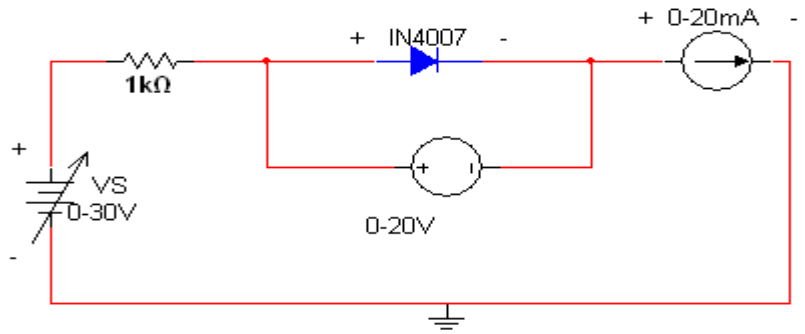
2. To find the static and dynamic forward bias resistance and reverse bias resistance.

## APPARATUS REQUIRED:-

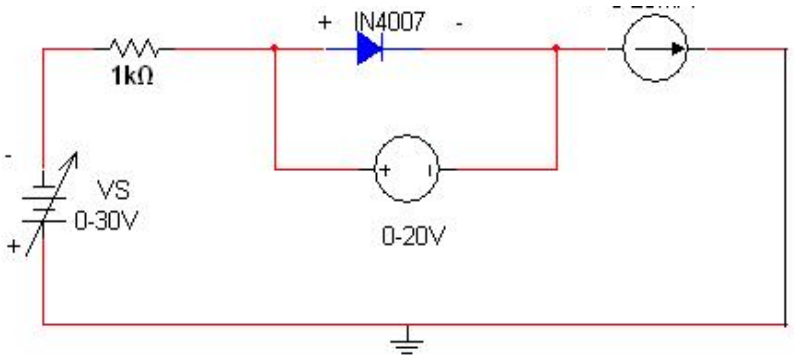
| | |
|---|---|
| 1. IN 4007 Diode (Silicon) | 1.No. |
| 2. OA79(Ge) | 1.No. |
| 3. Resistor 1KΩ | 1.No. |
| 4. 0-20 mA DC Ammeter | 1.No. |
| 5. 0-200 μA DC Ammeter | 1.No. |
| 6. 0-20 V DC Voltmeter. | 1.No. |
| 7. 0-30 V Regulated Power Supply | 1.No. |
| 8. Bread Board | 1.No |
| 9. Connecting wires | set |

## CIRCUIT DIAGRAMS:-

### FORWARD BIAS




### REVERSE BIAS



## THEORY:

A P-N Junction diode is also called as Semiconductor diode (Ge or Si). When a semi conductor is doped with p type impurity on one half and with N type impurity on the other half and heated to a temperature of $1200^0$C then a P-N Junction diode is formed. Junction diode can work in two types of biases.

## FORWARD BIAS:

When P-type (Anode) is connected to +ve terminal and n- type (cathode) is connected to –ve terminal of the supply voltage, is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward voltage due to majority carriers take part in conduction of current.

## REVERSE BIAS:

When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current is due to minority charge carriers.

## CUT IN VOLTAGE:

The Forward Voltage at which the current starts to rise abruptly is known as Cut –In voltage of the diode. For Ge is 0.3V, For Si is 0.7V.

## PROCEDURE:

## FORWARD BIAS CHARACTERISTICS:

1. Make the Circuit connection as per the Circuit Diagram on the bread board
2. The regulated Power supply is switched ON and the source voltage is slowly increased and the voltage across the PN Junction diode insteps of 0.1Volt is noted down and the Corresponding diode currents are noted down under forward bias Condition in table given below.
3. The graph $V_f$ versus $I_f$ is plotted on the graph Sheet to the scale.
4. The dynamic forward bias resistance of the diode is calculated from the graph

$$r = \frac{\Delta V}{\Delta I}$$

5. The cut in Voltage of the diode is observed and noted down.

**TABLE:**

**FORWARD BIAS CHARACTERISTICS**:

| S.N o | Forward Bias Voltage ($V_f$) in volts | | Forward Bias Current (If) in mA | |
|---|---|---|---|---|
| | **Ge** | **Si** | **Ge** | **Si** |
| 1 | | | | |
| 2 | | | | |
| 3. | | | | |
| 4. | | | | |
| 5. | | | | |
| 6. | | | | |
| 7. | | | | |

**REVESE BIAS CHARACTERISTICS:**

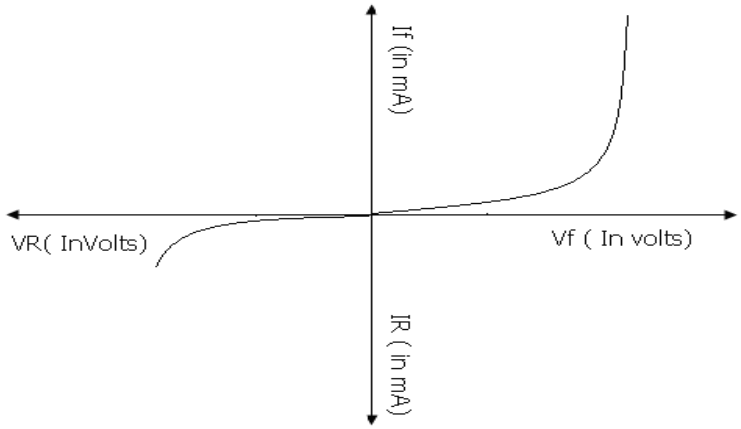
1. The Circuit is connected as per the Circuit Diagram on the bread board.
2. The regulated Power supply is switched on and the source voltage is slowly increased and the voltage across the PN Junction diode insteps of 1Volt is noted down and the Corresponding diode currents are noted down under reverse bias Condition in the table given below.
3. The graph Vr versus Ir is plotted on the graph Sheet to the scale.
4. the dynamic reverse bias resistance of the diode is calculated from the graph.

$$r = \frac{\Delta V}{\Delta I}.$$

**REVERSE BIAS CHARACTERISTICS**:

| S.N o | Reverse Bias Voltage (Vr) in Volts | | Reverse Bias Current (Ir) in μ A | |
|---|---|---|---|---|
| | **Ge** | **Si** | **Ge** | **Si** |
| 1 | | | | |
| 2 | | | | |
| 3. | | | | |
| 4. | | | | |
| 5. | | | | |
| 6. | | | | |
| 7. | | | | |
| 8. | | | | |
| 9. | | | | |
| 10. | | | | |

**MODEL GRAPH:**




**RESULT :**

The V-I Characteristics of the PN Junction diode are plotted for the Both forward and reverse bias conditions and Calculated the dynamic forward and reverse bias resistance.

**QUESTIONS:**

1. Define forward resistance and Reverse Resistance, What are the approximate values from the graph?
2. Define Cut in voltage of a diode, mention the cut in voltage for Ge & Si?
3. Explain the working of PN Junction in Forward and Reverse Bias conditions?
4. Define depletion region of a diode?
5. What is meant by transition & space charge capacitance of a diode?
6. Is the V-I relationship of a diode Linear or Exponential?
7. Define cut-in voltage of a diode and specify the values for Si and Ge diodes?
8. What are the applications of a p-n diode?

# 2. ZENER DIODE CHARACTERISTICS AND ZENER AS VOLTAGE REGULATOR

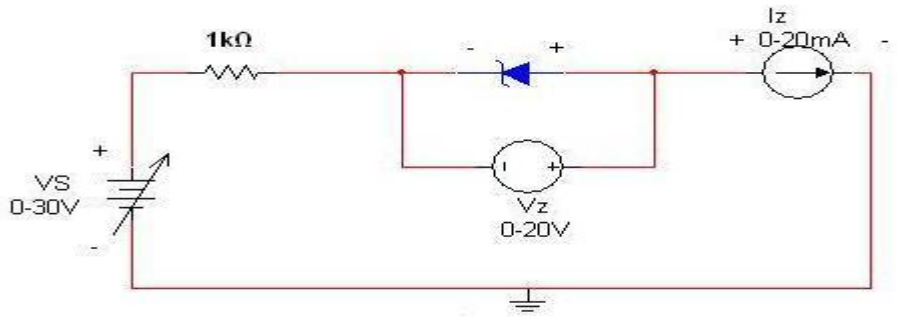
**AI M:-** To Obtain the Voltage – Current characteristics of a Zener diode and find out the Zener Break down Voltage from the Characteristics.

**APPARATUS REQUIRED:-**

1. D.C Regulated Power Supply 0-30V 1No.
2. Zener Diodes -3.9V,-8.2V Each 1No.
3. Resistor 1 KΩ & 680 Ω 1No.
4. DC Ammeter 0-20mA 1No.
5. DC Voltmeters 0-1V,0-10V Each 1No.
6. Decade Resistance Box 1No.
7. Bread Board. 1No.

**CIRCUIT DIAGRAMS:-**

**REVERSE BIAS CHARACTERISTICS:-**

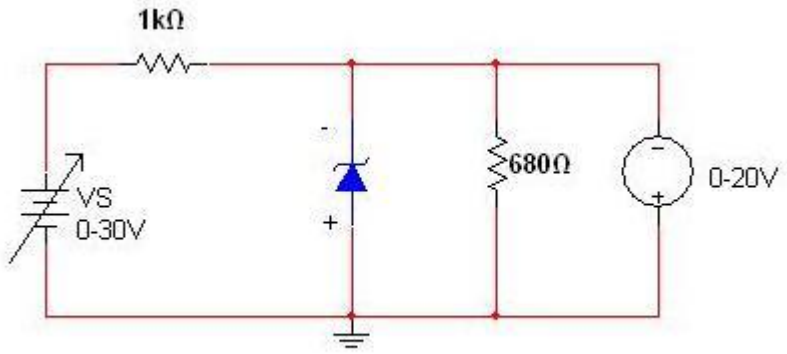



**TABULAR FORMS:-**

**CASE I. REVERSE BIAS CHARACTERISTICS:-**

| S.No | Source voltage(Vs) in volts | Zener diode voltage (Vz) in volts | Zener diode current (Iz) in mA |
|---|---|---|---|
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |
| 5 | | | |
| 6 | | | |
| 7 | | | |
| 8 | | | |
| 9 | | | |
| 10 | | | |
| 11 | | | |

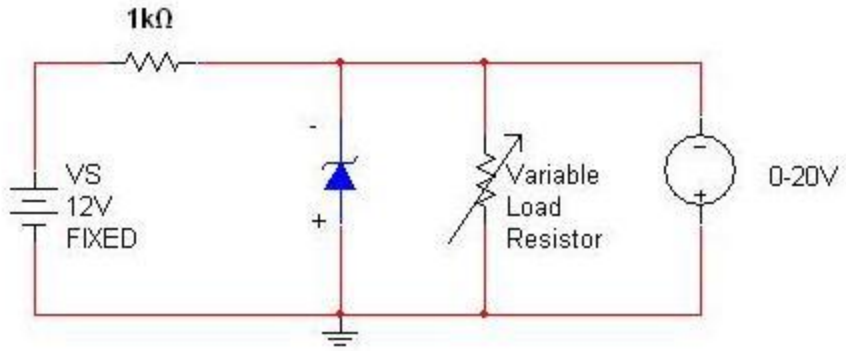
## CASE II . REGULATION WITH VARYING INPUT VOLTAGE :




## TABULAR COLUMN:

| S. No | Source Voltage(Vs) in Volts | Load voltage ($V_L$) in volts | Load Current ($I_L$)in mA $I_L = V_L / R_L$ |
|---|---|---|---|
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |
| 5 | | | |
| 6 | | | |
| 7 | | | |
| 8 | | | |

## CASE III .REGULATION WITH VARYING LOAD RESISTANCE :



**TABULAR COLUMN:**

| S.No | Load Resistance ($R_L$) in KΩ | Load Voltage($V_L$) in Volts | Load Current in mA $I_L = V_L / R_L$ |
|---|---|---|---|
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |
| 5 | | | |
| 6 | | | |
| 7 | | | |
| 8 | | | |

**THEORY :**

**CASE (I) :**

The Diodes which are designed with adequate power dissipation to operate in the break down region are known as Break Down (or) Zener diodes. These diodes are employed as constant voltage sources.

**CASE (II) :**

a) As the input voltage increases, the input current also increases. This increase the current through the Zener Diode with out affecting the load current.
b) The increase in the input current will also increases the voltage drop across the series resistance ($R_L$), thereby keeping the load voltage ($V_L$) as constant.

**CASE (III) :**

a) When the load resistance decreases the load current increases.
b) This causes the Zener current to decrease. As a result of this the input current and voltage drop across series resistance remains constant. Thus the load voltage is kept constant.

**PROCEDURE:-**

**CASE(I) : Reverse bias characteristics**

1. Make the connections as per the circuit diagram.
2. Switch the DC Regulated power supply and slowly increase the source Voltage and note down the Voltage across Zener diode insteps of the 1Volt and note the Corresponding diode current as per table given below.
3. Repeat the above procedure for the 9.1V Zener diode.
4. Plot the graph between Voltage across the Zener diode (Vr) Vs current (Ir) through the diode on graph sheet for the both zener Diodes.

## CASE (II): REGULATION WITH VARYING INPUT VOLTAGE

1. Make the connections as per the circuit diagram.
2. Keep the input voltage from 0 – 10V in steps of 1 V and note down the readings of source
3. voltage ( $V_s$) , Load voltage ($V_L$) , Load current ($I_L$) . c) Plot the graph between $I_L$ Versus $V_L$.

## CASE(III) : REGULATION WITH VARYING LOAD RESISTANCE

1. Make the connections as per the circuit diagram
2. Keep the input voltage constant at 12V and note down the current without load resistance. Note this as No load voltage.
3. Slowly vary the load resistance in steps of 1KΩ to up to 10KΩ and note down the corresponding meter readings. Calculate the regulation by using the formula.

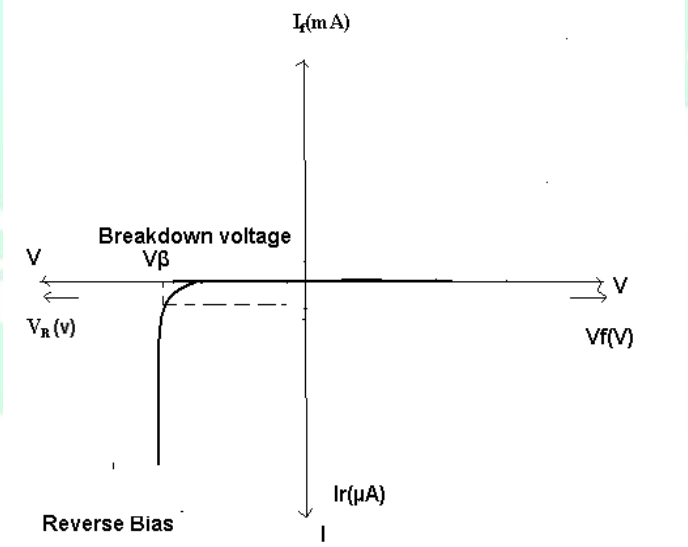
$$(V_{NL} - V_{FL}) / V_{FL}$$

4. Plot the graph between $I_L$ Versus $V_L$.

## ZENER BREAK DOWN VOLTAGE:-

Draw the tangent on the reverse bias Characteristics of the Zener Diode starting from the Knee and touching most of the points of the Curve.
The point where the Tangent intersects the X-axis is the Zener Break down Voltage.

## MODEL GRAPH:-




**RESULT:-** The V- I Characteristics of the Zener Diode and the Zener Break Down Voltage from the Characteristics are Observed.

**QUESTIONS:**

1. What type of temp? Coefficient does the zener diode have?
2. If the impurity concentration is increased, how the depletion width effected?
3. Does the dynamic impendence of a zener diode vary?
4. Explain briefly about avalanche and zener breakdowns?
5. Draw the zener equivalent circuit?
6. Differentiate between line regulation & load regulation?
7. In which region zener diode can be used as a regulator?
8. How the breakdown voltage of a particular diode can be controlled?
9. What type of temperature coefficient does the Avalanche breakdown has?
10. By what type of charge carriers the current flows in zener and avalanche breakdown diodes?

# 3. RECTIFIER WITHOUT FILTERS (HALFWAVE & FULLWAVE)

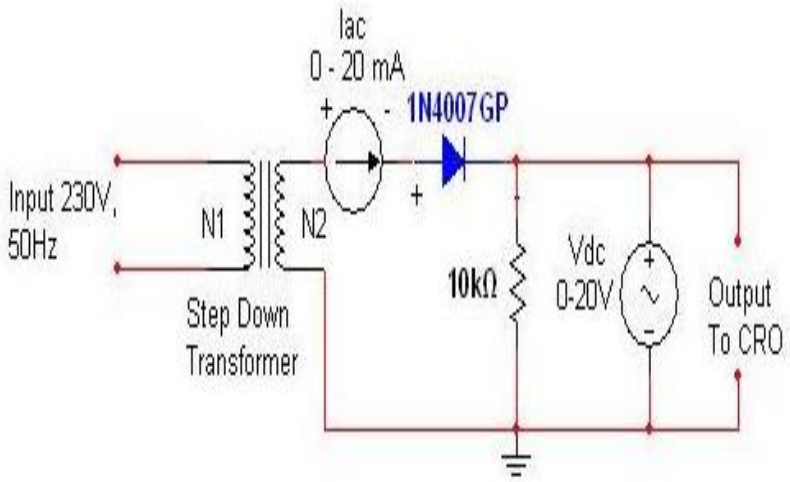
**AIM:** To rectify the signal and then to find ripple factor, efficiency and percentage of regulation in full wave and half wave rectifier without filters.

**APPARATUS:**

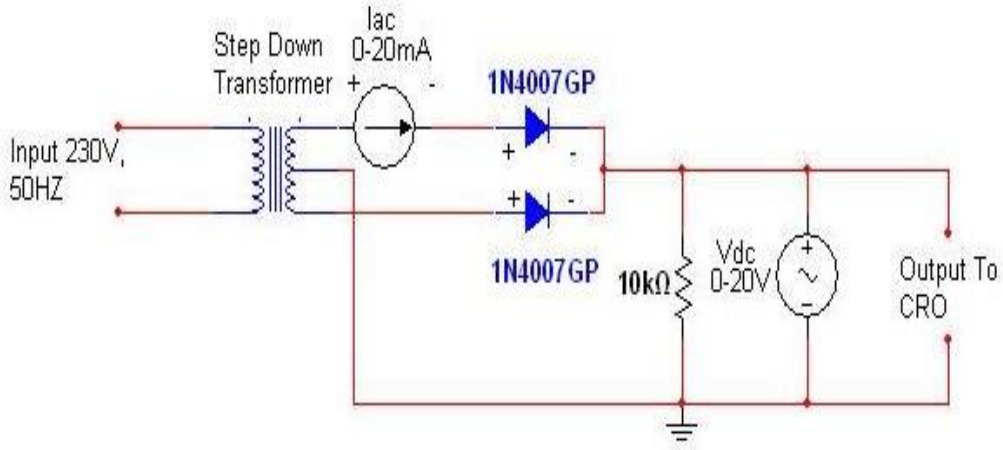
1. Transformer 230v / 6v – 0 – 6v
2. Diodes IN4007 2 No
3. R esistance 10k
4. Multimeter
5. Bread Board
6. 20MHz Dual Trace CRO
7. Connecting wires

**CIRCUIT DIAGRAM:**

**HALFWAVE RECTIFIER:**




**FULLWAVE RECTIFIER:**



## THEORY:

A Half wave Rectifier is one which converts the ac voltage in to a pulsating dc voltage using only one half cycle of the applied voltage. Rectifier conducts during one half cycle only. During positive half-cycle of the input voltage, the diode D1 is in forward bias and conducts through the load resistor R1. Hence the current produces an output voltage across the load resistor R1, which has the same shape as the +ve half cycle of the input voltage.

During the negative half-cycle of the input voltage, the diode is reverse biased and there is no current through the circuit. i.e, the voltage across R1 is zero. The net result is that only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified o/p voltage is the value measured on dc voltmeter.

For practical circuits, transformer coupling is usually provided for two reasons.

1. The voltage can be stepped-up or stepped-down, as needed.
2. The ac source is electrically isolated from the rectifier. Thus preventing shock hazards in the secondary circuit.

## PROCEDURE:

### COMMON TO HALFWAVE RECTIFIER & FULLWAVE RECTIFIER:

1. Connecting the circuit on bread board as per the circuit diagram
2. Connect the primary of the transformer to main supply i.e. 230V, 50Hz
3. Connect the Multimeter at output terminals and note down the Vrms and Vdc as per given tabular form.
4. Disconnect load resistance and note down No load voltage Vdc.
5. Connect Channel – II of CRO at output terminals and CH – I of CRO at Secondary Input terminals observe and note down the Input and Output Wave form on Graph Sheet

## CALCULATIONS:

1. Calculate Ripple Factor $\gamma = \frac{Vrms}{Vdc}$

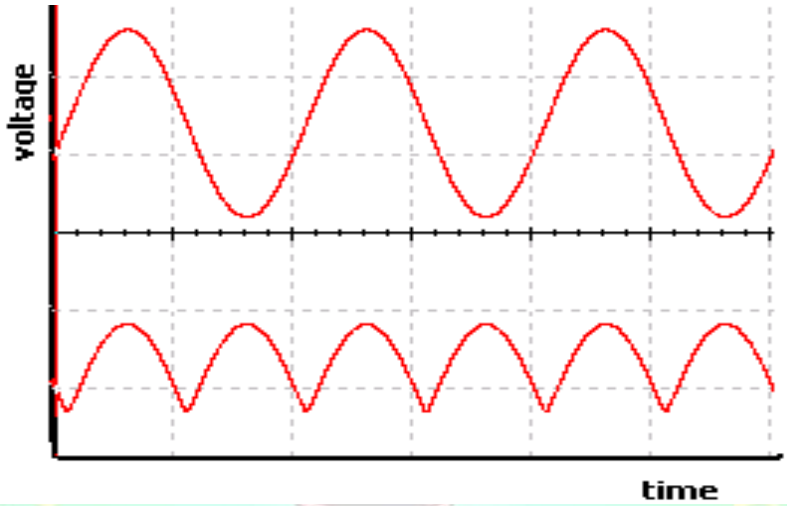
2. Calculate Percentage of regulation = $\frac{Vnoload - Vfull\ load}{Vfull\ load} \times 100\%$

3. Calculate efficiency $\eta = P_{dc} / P_{ac}$

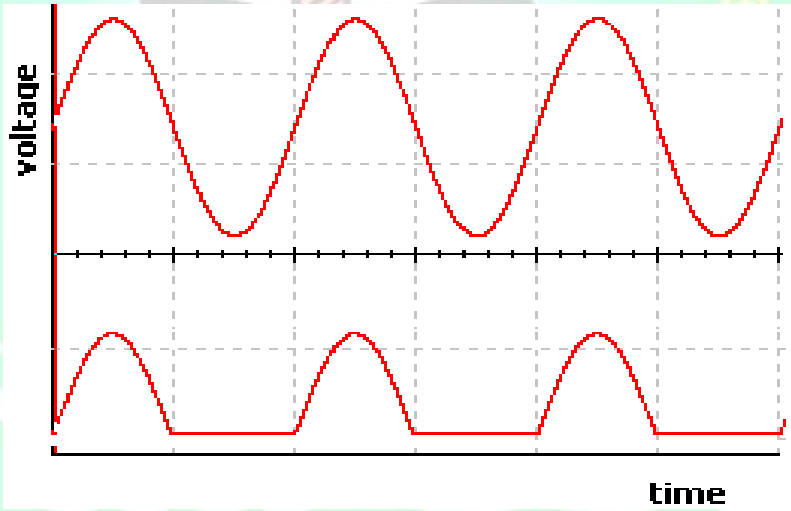
   $P_{dc} = V_{dc} \times I_{dc} = V_{dc}^2 / R_L$

   $Pac = Vac \times Iac$

**WAVE SHAPES:**




**FULL WAVE WITHOUT FILTER**




**HALF WAVE WITHOUT FILTER**

**RESULT:**

Observe Input and Output Wave forms and Calculate ripple factor and percentage of regulation in Full wave and half wave rectifiers without filter.

**QUESTIONS:**

1. What is the PIV of Half wave rectifier?
2. What is the Ripple factor, efficiency, % of Regulation o f Rectifier?
3. What is the rectifier?
4. What is the difference between the half wave rectifier and full wave Rectifier?
5. What is the o/p frequency of Bridge Rectifier?
6. What are the ripples?
7. What is the function of the filters?
8. What is TUF?
9. What is the average value of o/p voltage for HWR?
10. What is the peak factor?

# 4. RECTIFIER WITH FILTERS (HALFWAVE & FULLWAVE)

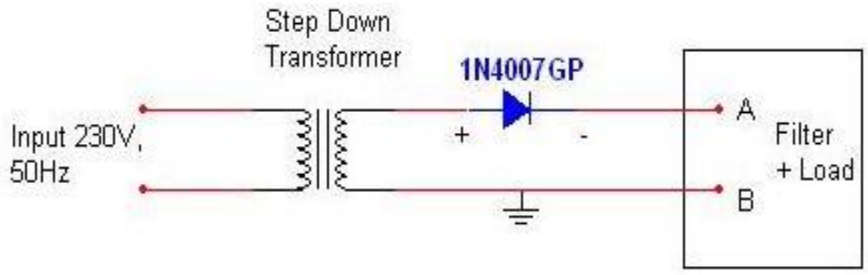
**AIM:** To rectify the signal and then to find ripple factor in full wave and half wave rectifier with filters.

**APPARATUS:**

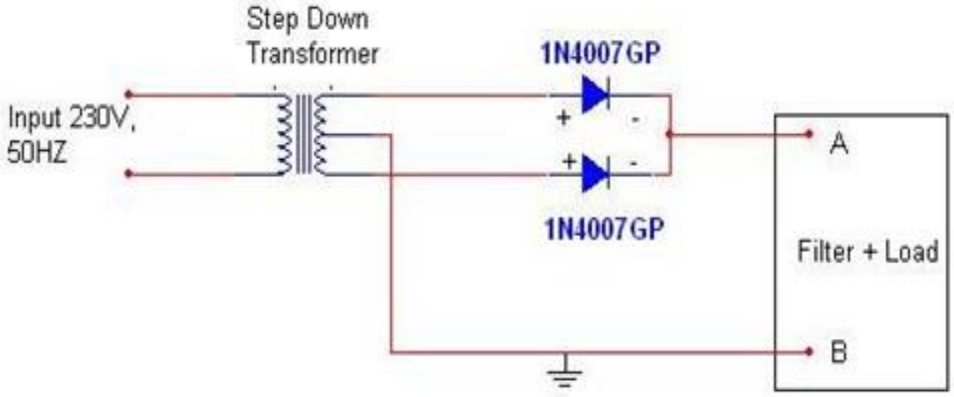
1 .Transformer 230v/6v – 0 – 6v
2. Diodes IN4007 - 2 no's
3 . Capacitor 470µf/35v - 1 no.
4 . Decade Inductance Box
5. Resistance 1K
6. Multi meter
7 . Bread Board
8. 20MHz Dual Trace CRO
9. Connecting wires

**CIRCUIT DIAGRAM:**

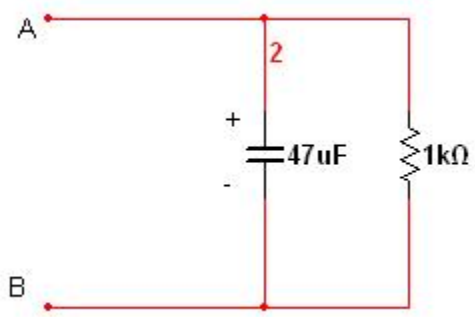
**HALFWAVE RECTIFIER:**



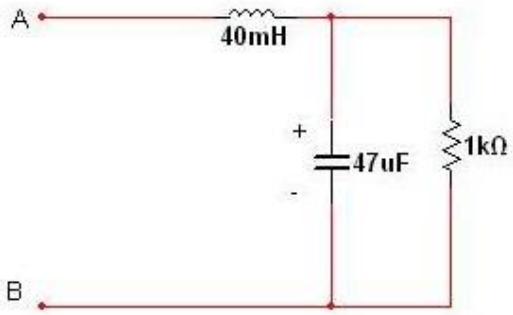

**FULLWAVE RECIFIER :**



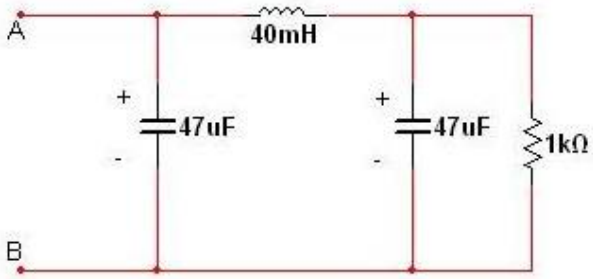
**C – FILTER:**




**L-C FILTER:**




**CLC – FILTER:**




**PROCEDURE:**

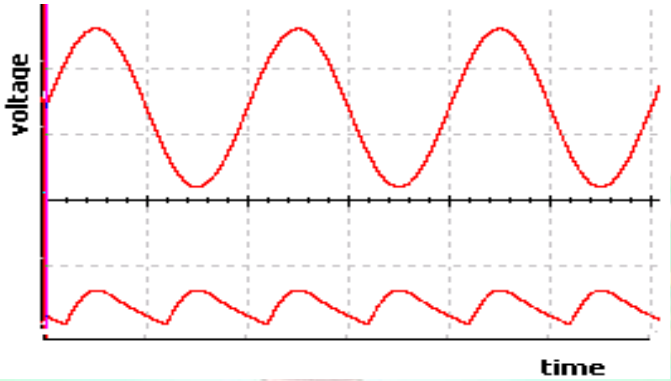
**FULLWAVE RECTIFIER:**

1. Make the connections as per the circuit diagram
2. Make the connection of primary transformer to main supply i.e. 230V, 50Hz
3. Make the connection of decade resistance box and set the $R_L$ value to 100Ω
4. Make the connection of multimeter at output terminals and vary the load resistance (DRB) from 100Ω to 5KΩ and note down the Vac and Vdc as per given tabular form
5. Disconnect load resistance ( DRB) and note down No load voltage Vdc
6. Make the connection of load resistance at 100KΩ and connect CH – I of Dual Trace CRO at Secondary (Input) terminals, Channel – II of Dual Trace CRO at output terminals and observe and note down the Input and Output Wave form on Graph Sheet

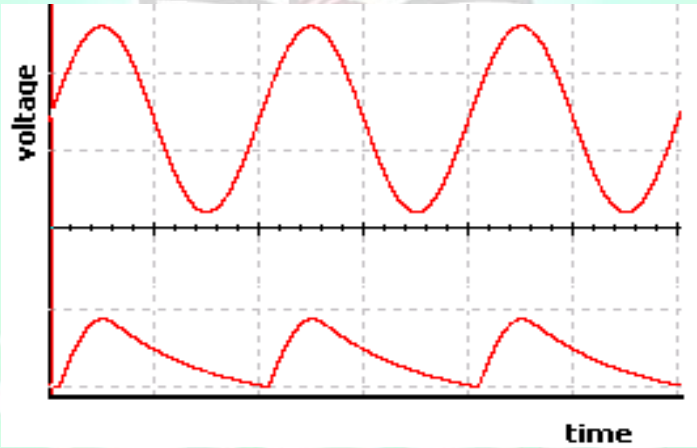
**HALFWAVE RECTIFIER:**

7. Make the connections as per the circuit diagram and repeat the above procedure from steps 2 to 6 Calculate Ripple Factor $\gamma = V_{rms} / V_{dc}$

**WAVE SHAPES:**




**FULL WAVE WITH FILTER**




**HALF WAVE WITH FILTER**

**RESULT:** Observe Input and Output Wave forms and Calculate ripple factor and percentage of regulation in Full wave and Half wave rectifiers with capacitor filter

**QUESTIONS:**

1. What is the need of filter?
2. Why we are using L & C components in the filter?
3. What are the types of filters?
4. Which is the best among the different types of filters?

# 5. RC PHASE SHIFT OSCILLATOR

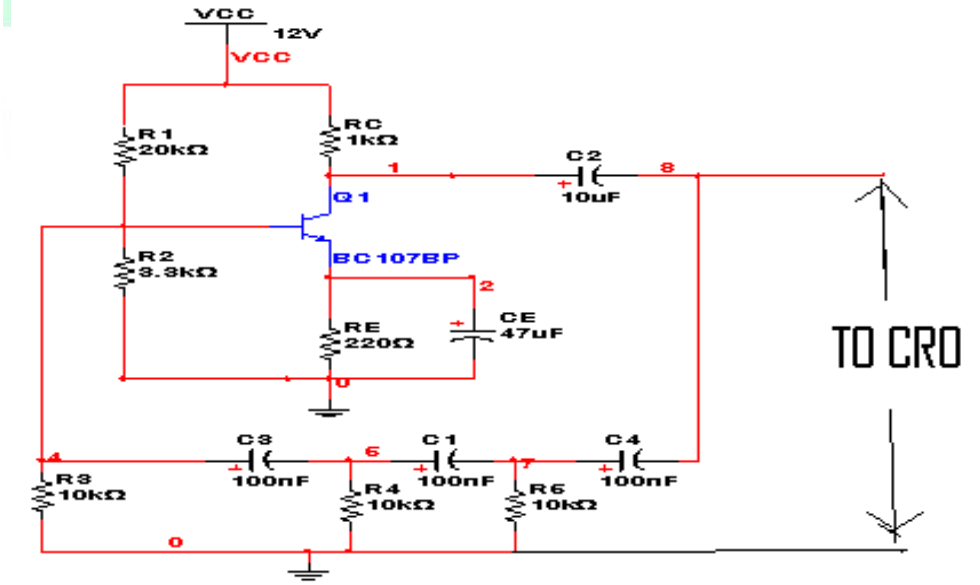
## AIM:

To design and simulate RC Phase Shift Oscillator to generate a sinusoidal waveform of desired frequency using BJT amplifier.

## APPARATUS:

1. Regulated power supply - 1 No.
2. Function generator - 1 No.
3. CRO - 1 No.
4. Transistor (BC 107BP) - 1 No.
5. Resistors (3.3 KΩ, 10KΩ, 1KΩ, 1.5 KΩ,) - 1 No. each
6. Resistor (2.2KΩ) - 3 No. each
7. Capacitors (0.1 μF, 10 μF) - 3,1 No. each
8. Bread Board - 1 No.
9. Connecting wires.

## CIRCUIT DIAGRAM:




## THEORY:

RC phase shift oscillator or simply RC oscillator is a type of oscillator where a simple RC network (resistor-capacitor) network is used for giving the required phase shift to the feedback signal. In LC oscillators like Hartley oscillator and Colpitts oscillator an LC network (inductor-capacitor network) is used for providing the necessary positive feedback. The main feature of an RC phase shift oscillator is the excellent frequency stability. The RC oscillator can output a pure sine wave on a wide range of loads.

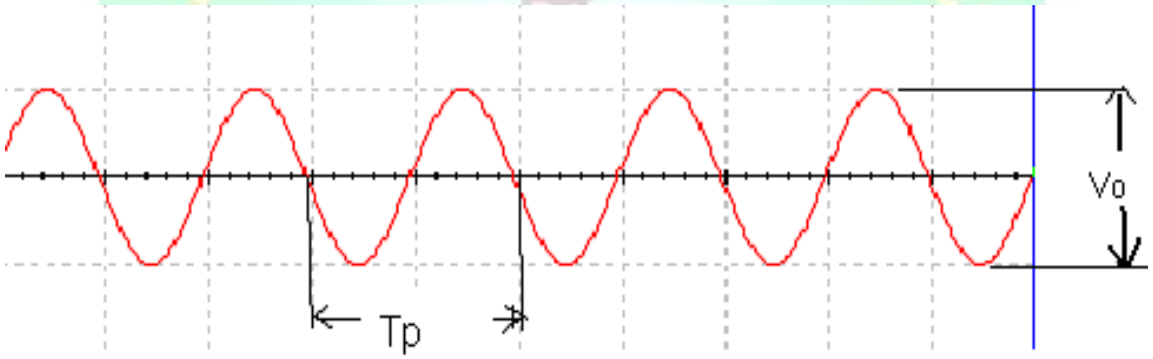
## PROCEDURE:

1. Connect the circuit diagram as shown in the figure.
2. Measure the time period of the waveform obtained on CRO & Calculate the frequency of oscillations.
3. Repeat the procedure for different values of capacitance.

## OBSERVATIONS:

| Value of R,C | Theoretical Frequency | Observed Frequency | Signal Amplitude |
|---|---|---|---|
| 10KΩ,0.1 μF | | | |
| 1K Ω, 0.01 μF | | | |

## EXPECTED WAVEFORM:




## RESULT:

For a given Circuit of RC Phase Shift Oscillator the sine Wave of _____frequency is observed.

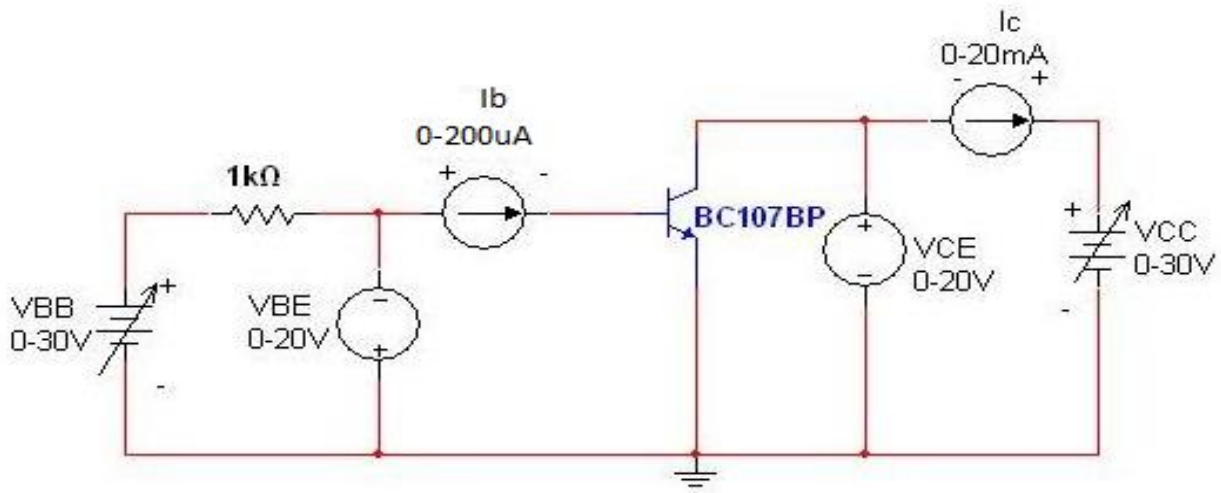
# 6. INPUT & OUTPUT CHARACTERISTICS OF TRANSISTOR IN CE CONFIGURATION

**AIM: To** Plot the Family of input and output Characteristics of a Transistor connected in Common Emitter Configuration.

## APPARATUS REQUIRED:

| | |
|---|---|
| 1. Transistor BC 107 | 1No. |
| 2. Resistor 1KΩ | 1.No. |
| 3. Connecting Wires | 1 Set |
| 4. Ammeter 0-20mA, 0-500 μ A | 1 Each |
| 5. Multimeter | 1No. |
| 6. 0-30,1A Dual Channel power supply. | 1.No. |
| 7. Bread Board | 1No. |

## CIRCUIT DIAGRAM:




## THEORY:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals . Therefore the emitter terminal is common to both input and output. The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement IB increases less rapidly with VBE . Therefore input resistance of CE circuit is higher than that of CB circuit.

The output characteristics are drawn between $I_c$ and $V_{CE}$ at constant $I_B$. The collector current varies with VCE unto few volts only. After this the collector current becomes almost constant, and independent of $V_{CE}$. The value of $V_{CE}$ up to which the collector current changes with $V_{CE}$ is known as Knee voltage. The transistor always operated in the region above Knee voltage, $I_C$ is always constant and is approximately equal to $I_B$.

**PROCEDURE**:

**INPUT CHARACTERISTICS**

1. Make the connections as per the circuit diagram.
2. Make $V_{CE}$ Open and Vary the 5 V Supply (Channel 1) and note the Values of $I_B$ and $V_{BE}$, by increasing the $I_B$ in Steps of .5mA.
3. Adjust $V_{CE}$ = 1V in Channel 2 Power supply.
4. Vary the 0-5V (Channel 1) power Supply and note the Values of $I_B$ and $V_{BE}$
5. Repeat the Steps 3 and 4 for $V_{CE}$ = 2V ,3V,4V.
6. Need not connect 0-2mA($I_C$ Measurement), Ammeter while taking the input Characteristics.

**TABULAR FORM:**

| S.No | VCE = 0V | | VCE = 3V | | VCE = 6V | |
|---|---|---|---|---|---|---|
| | VBE(V) | IB(uA) | VBE(V) | IB(uA) | VBE(V) | IB(uA) |
| 1 | 0.1 | | 0.1 | | 0.1 | |
| 2 | 0.2 | | 0.2 | | 0.2 | |
| 3 | 0.3 | | 0.3 | | 0.3 | |
| 4 | 0.4 | | 0.4 | | 0.4 | |
| 5. | 0.5 | | 0.5 | | 0.5 | |
| 6 | 0.6 | | 0.6 | | 0.6 | |
| 7. | 0.7 | | 0.7 | | 0.7 | |
| 8 | 0.8 | | 0.8 | | 0.8 | |

**OUTPUT CHARACTERISTICS:**

1. Make the connections as per the circuit diagram.
2. Connect 0-500 μ A Ammeter in place of 0-20mA.
3. Adjust 0-5V (Channel -1) power Supply and fix the Values of $I_B$ = 10 μ A
4. Vary the $V_{CE}$ 0-20V (Channel -2) power supply and note down the Values of the Ic and $V_{CE}$. Vary in the Steps of 1V.
5. Repeat the steps 3 & 4 for $I_B$ = 30 μ A, 40 μ A, 50 μ A .

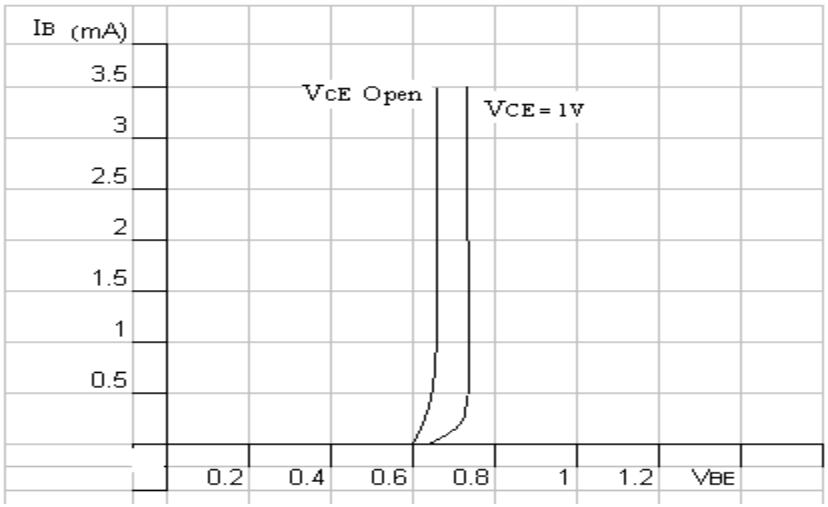
**TABULAR FORM:**

1. Plot the input characteristics by taking IB on Y-Axis and $V_{BE}$ on X-Axis.
2. Plot the output characteristics by taking IC on the Y-Axis and VCE on X –Axis

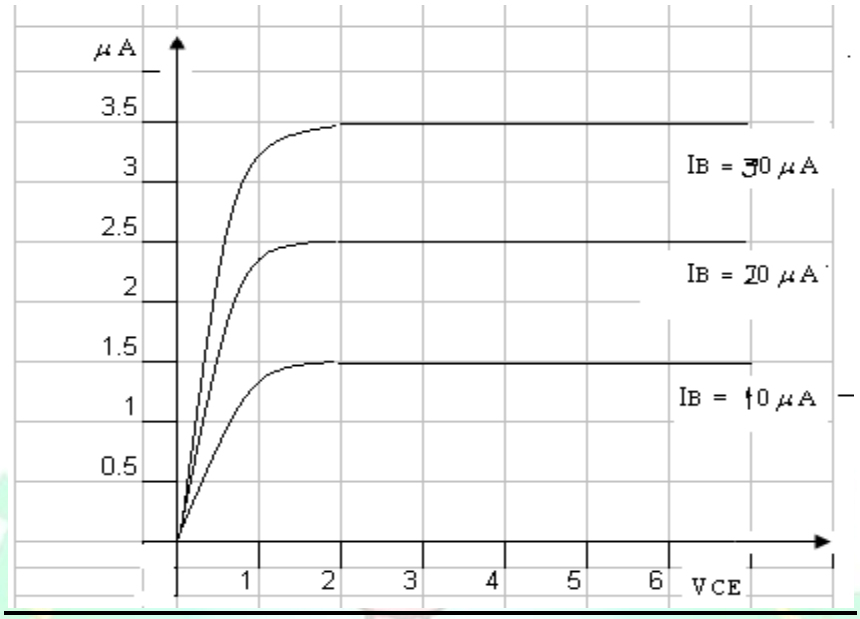
| S.No | $I_B$ = 10 uA | | $I_B$ = 20 uA | | $I_B$ = 30 uA | |
|---|---|---|---|---|---|---|
| | $V_{CE}$(mA) | Ic(mA) | $V_{CE}$(mA) | Ic(mA) | $V_{CE}$(mA) | Ic(mA) |
| 1 | 1 | | 1 | | 1 | |
| 2 | 2 | | 2 | | 2 | |
| 3 | 3 | | 3 | | 3 | |
| 4 | 4 | | 4 | | 4 | |
| 5 | 5 | | 5 | | 5 | |
| 6 | 6 | | 6 | | 6 | |
| 7 | 7 | | 7 | | 7 | |
| 8 | 8 | | 8 | | 8 | |
| 9 | 9 | | 9 | | 9 | |
| 10 | 10 | | 10 | | 10 | |

Input Impedance hie = $\Delta V_{BE} / \Delta I_B$ at $V_{CE}$ constant
Output impedance hoe = $\Delta V_{CE} / \Delta I_C$ at $I_B$ constant
Reverse Transfer Voltage Gain hre = $\Delta V_{BE} / \Delta V_{CE}$ at $I_B$ constant
Forward Transfer Current Gain hfe = $\Delta I_C / \Delta I_B$ at constant $V_{CE}$

## GRAPH: INPUT CHARACTERISTICS



## OUTPUT CHARACTERISTICS:



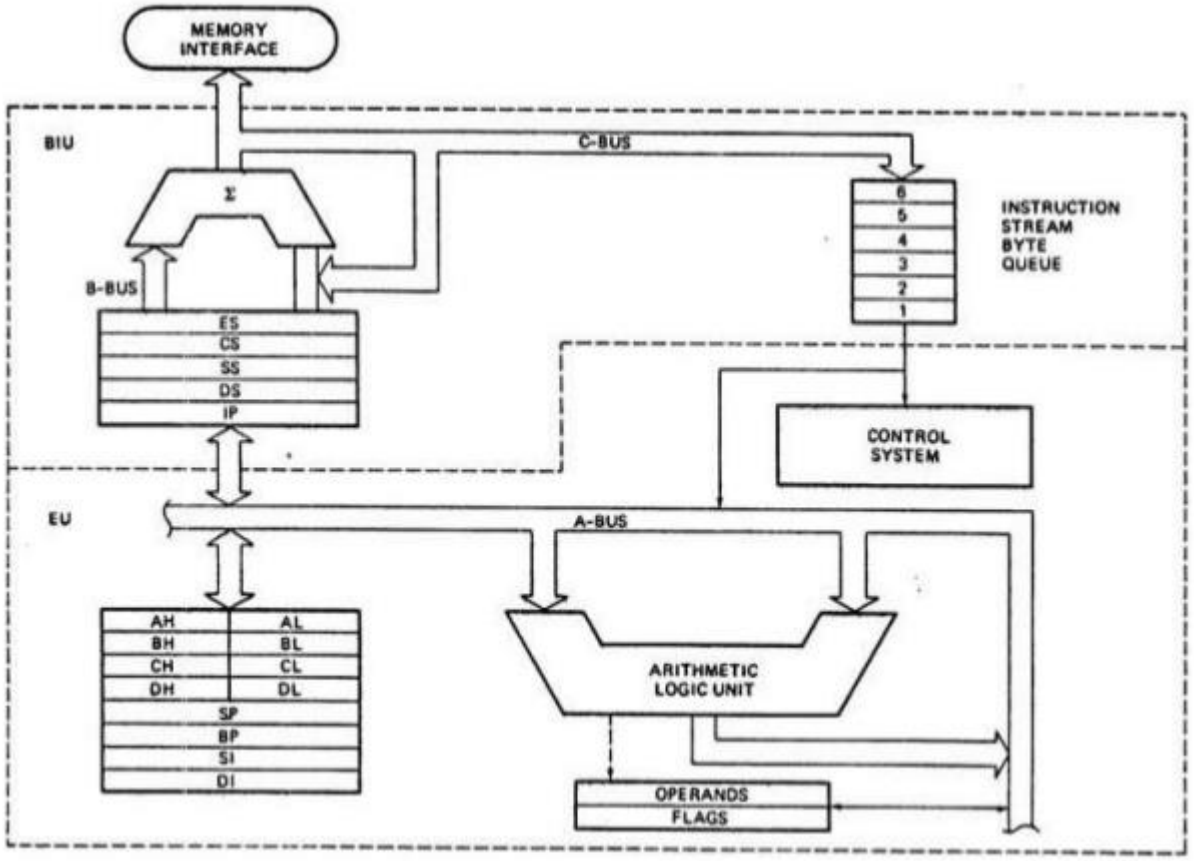

## RESULT:

Input and output characteristics of CE are plotted.

## QUESTIONS:

1. What is meant by $\alpha$ *and* $\beta$ in a CE transistor Characteristics?
2. What are the input and output impedances of CE configuration?
3. Identify various regions in the output characteristics?
4. what is the relation between $\alpha$ *and* $\beta$?
5. Define current gain in CE configuration?
6. Why CE configuration is preferred for amplification?
7. What is the phase relation between input and output?
8. Draw diagram of CE configuration for PNP transistor?
9. What is the power gain of CE configuration?
10. What are the applications of CE configuration?

## 7.Introduction to 8086/8088 Microprocessor




1. General Facilities - BIU and EU - Data Registers - Segment Registers - Index Registers - Pointer Registers - Flag Register - Memory Addressing - Physical Memory Address Calculations.
2. 8086 – Introduction • 16 bit µp with 20 bit address bus & 16 bit data bus • Can address up to 220 = 1 MB memory directly • Can read or write 8 or 16 bit data • 8088 - 8 bit data bus • Internal architecture has two main units • BIU - Bus Interface Unit • EU – Execution Unit
3. • BIU and EU work simultaneously for instruction execution and form 2 stage instruction pipeline. • BIU – has bus interface logic, segment registers, memory addressing logic and 6 byte instruction queue. • While EU is busy in instruction execution, BIU fetches instruction from memory and stores them in instruction queue.
4. If EU executes a jump instruction – Program control to be transferred to another location then BIU • Resets the queue • Fetches instruction from new address • Passes the instruction to EU • Starts refilling the queue from new location • Process is called pipeline flushing.
5. . BIU of 8088 • 8088 – 4 byte instruction queue • Each time there is empty space of 2 bytes or more 8086 BIU startes filling the queue. • 8088 BIU fills the queue when there is empty space of 1 byte.
6. . Execution Unit (EU) • Contains – instruction decoder, ALU, general purpose registers, pointer registers, index registers, flag register and control circuitary to execute instruction. • EU is resposible for- – Execution of instructions – Providing address to BIU for fetching data/instruction. – Manipulating various registers as well as flag register. • EU is almost

completly isolated from outside world. • BIU performs all bus operations for EU. • Overlapped fetching and execution of instruction is shown

7. It is assumed that • Two µps i.e 2nd generation and 8086 execute the instruction in same no. of clock cycles. • Due to overlapping of fetch and excute, 8086/8088 is able to excute 3 instruction in lesser time but also able to fetch 4th and 5th instruction. • Register Set- 8086 has fourteen – 16 bit registers • Data Registers • Segment Registers • Pointer & index register • flag register
8. Data Registers- Four sixteen bit AX,BX,CX,DX • Or 8 – 8 bit registers • AH AL BH BL CH CL DH DL • AX- Primary Accumulator • Input-Output operations through AX(or AL) • Several string operations require one operand to be in AX (or AL). • 16 bit divide or multiply - AX has one word operand (AL for 8 bit operation). • 32 bit multiply or divide – AX holds lower order word operand.
9. .BX – GPR (Genral Purpose Register) + Base Register • CX – GPR + Count Register in multi iteration instruction. • DX – GPR + used in I/O instructions, multiply & divide instructions.
10. Segment Registers • concept of memory segmentation. Memory divided into no. of parts called segments. • In 8086, 1 MB physical memory can be divide into 4 types of segments. • Starting address of each segment is placed in 16 bit register • CS – Code Segment Register. • DS – Data Segment Register. • SS – Stack Segment Register. • ES – Extra Segment Register. • Each segment has memory space of 64k byte
11. Index Registers SI – Source Index Register DI – Destination Index Register • May be used as GPR. However main purpose is to store address offset in case of – Indexed, Base Indexed, and Relative Base Indexed addressing modes
12. . Pointer Registers • Stack Pointer(SP) - provides access to stack top. Holds offset address of stack top. • Instruction Pointer(IP) - holds offset address of next instruction to be executed. Like program counter. • Base Pointer (BP) - GPR. Main purpose is to provide indirect access to data in stack.
13. Flag Register - also called program status word (PSW) 9 active Flags 6 status flags 3 control flags
14. .Status Flag – • Carry – Arithmetic operation results is carry out of MSB or Borrow in Subtraction. Also used in shift & Rotate. • Parity – Even parity in byte operation or lower byte of word operation • Auxiliary Carry – set if there in carry out of lower nibble to higher nibble in 8 bit quantity or lower byte to higher byte in 16 bit quantity. Used in BCD operations. • Zero – set when result of operation is zero.
15. Sign – set when after arithmetic or logic operation, MSB of result = 1 indicates that result is negative. • Overflow – used to detect magnitude overflow in signed arithmetic. • For addition operation – flag is set when there is carry in to MSB but no carry out of MSB or vice versa. • For subtraction – flag is set when MSB needs a borrow but there is no borrow from MSB or vice versa.
16. Control Flags – • Direction – Used with string operations. When set (i.e = 1) then string operation in auto decrement mode (i.e right to left) when reset (i.e = 0) then string operation in auto increment mode (left to right) Interrupt Enable – • When = 1, enables 8086 to recognize external interrupts. When = 0, all maskable interrupts are disabled. No effect on non maskable interrupts. • Trap flag – when = 1, sets processor in single step mode for debugging.
17. . Memory Addressing – Real Mode • Real Mode – limited to 1 MB of memory i.e real memory. • Segment Register – 16 bits in length. • Memory address – 20 bits. • Segment register content are appended with 0000 to make it 20 bit address i.e segment register contents are multiplied by 16 • Now the address represent the starting address of segment in memory • Let us say CS = 1234H • After appending with 0000(=0H) we get 12340H as starting address of code segment in memory. • The size of a segment i.e 64kb i.e FFFFH • The address range of code segment 12340H to (12340 + FFFF) = 2233FH

18. A segment must thus start at 16 byte boundary [since last 4 bits = 0000] • Two segment can overlap with each other partially if segment address have been defined like that. • There may be more then one segment of a particular type. For that segment register contents are dynamically changed. • All real mode memory addresses consist of segment address plus an offset address. • Offset address – increment from starting of segment.
19. . Thus segment address defines the starting address of 64k byte memory segment. • Offset address selects a location within 64k byte memory segment. • Offset address is also known as logical address. • Physical address is actual memory location of operands = segment address appended with 0H + offset address = (segment address) x 16 + offset address.
20. .Let us take an example. -> Segment register = 1234H -> Offset = 0022H Physical address ? Segment starting address = 12340H + offset = 0022H _____ Physical address = 12362H Exercise 1 – calculate last address of segment, given the segment register values as 1234H, 2300H and AB00H.
21. Exercise -2 – Given physical address of memory location and segment register content, find the logical address i.e offset
22. . Note – • 8086 and 8088 operate only in real mode • 80286 – 80486 – Pentium – operate in real or protected mode. • Real mode operation allows microprocessor to address only first 1 MB of memory space even if it is 80486 µp. • Memory segmentation allows program to be relocated in any portion of memory.
23. . • There is a set combination of segment register and offset register known as default combination . Segment offset Special purpose CS IP Instruction address SS SP or BP stack address DS BX,DI,SI Data address An 8 or 16 bit number ES DI for string string destination instruction address.

# 8. ADDITION OF 2 8-BIT NUMBERS

**Aim: Write an assembly language program to Add two 8- bit hexa decimal Numbers?**

```
        MOV SI, 8000H
        MOV DI, 9000H
        MOV CL, 00
        MOV AL, [SI]
        INC SI
        MOV BL, [SI]
        ADD AL, BL
        JNC LABLE
        INC CL
LABLE:  MOV [DI], AL
        INC DI
        MOV [DI], CL
        INT 03……end of the program
```

OBSEVATION TABLE

| SL.NO | INPUT | | OUTPUT | |
|---|---|---|---|---|
| | 8000 | 8001 | 9000 | 9001 |
| 1 | | | | |
| 2 | | | | |

RESULT:

# 9. SUBTRACTION OF 2 8-BIT NUMBERS

**Aim: Write an assembly language program to Subtract two 8- bit hexa decimal Numbers?**

```
        MOV SI, 8000H
        MOV DI, 9000H
        MOV CL, 00
        MOV AL, [SI]
        INC SI
        MOV BL, [SI]
        SUB AL, BL
        JNB LABLE
        INC CL
        NOT AL
        ADD AL, 01
LABLE:  MOV [DI], AL
        INC DI
        MOV [DI], CL
        INT 03……end of the program
```

OBSEVATION TABLE

| SL.NO | INPUT | | OUTPUT | |
|---|---|---|---|---|
| | 8000 | 8001 | 9000 | 9001 |
| 1<br>2 | | | | |

RESULT

# 10. MULTIPLICATION OF 2 8-BIT NUMBERS

**Aim: Write an assembly language program to multiply two 8- bit hexa decimal Numbers?**

```
        MOV SI, 8000H
        MOV DI, 9000H
        MOV CL, 00
        MOV AL, [SI]
        INC SI
        MOV BL, [SI]
        SUB AL, BL
        JNB LABLE
        INC CL
        NOT AL
        ADD AL, 01
LABLE:  MOV [DI], AL
        INC DI
        MOV [DI], CL
        INT 03……end of the program
```

OBSEVATION TABLE

| SL.NO | INPUT | | OUTPUT | |
|---|---|---|---|---|
| | 8000 | 8001 | 9000 | 9001 |
| 1<br>2 | | | | |

RESULT

# 11. DIVISION OF 2 8-BIT NUMBERS

**Aim: Write an assembly language program to Divide two 8- bit hexa decimal Numbers?**

```
        MOV SI, 8000H
        MOV DI, 9000H
        MOV CL, 00
        MOV AL, [SI]
        INC SI
        MOV BL, [SI]
        SUB AL, BL
        JNB LABLE
        INC CL
        NOT AL
        ADD AL, 01
LABLE:  MOV [DI], AL
        INC DI
        MOV [DI], CL
        INT 03……end of the program
```

OBSEVATION TABLE

| SL.NO | INPUT | | OUTPUT | |
|---|---|---|---|---|
| | 8000 | 8001 | 9000 | 9001 |
| 1<br>2 | | | | |

RESULT

MALLA REDDY ENGINEERING COLLEGE
mrec
ज्ञानमेव शक्तिः

MALLA REDDY ENGINEERING COLLEGE
mrec
ज्ञानमेव शक्तिः

MALLA REDDY ENGINEERING COLLEGE
mrec
ज्ञानमेव शक्तिः

MALLA REDDY ENGINEERING COLLEGE
mrec
ज्ञानमेव शक्तिः

MALLA REDDY ENGINEERING COLLEGE
mrec
ज्ञानमेव शक्तिः